circuits manufacturing

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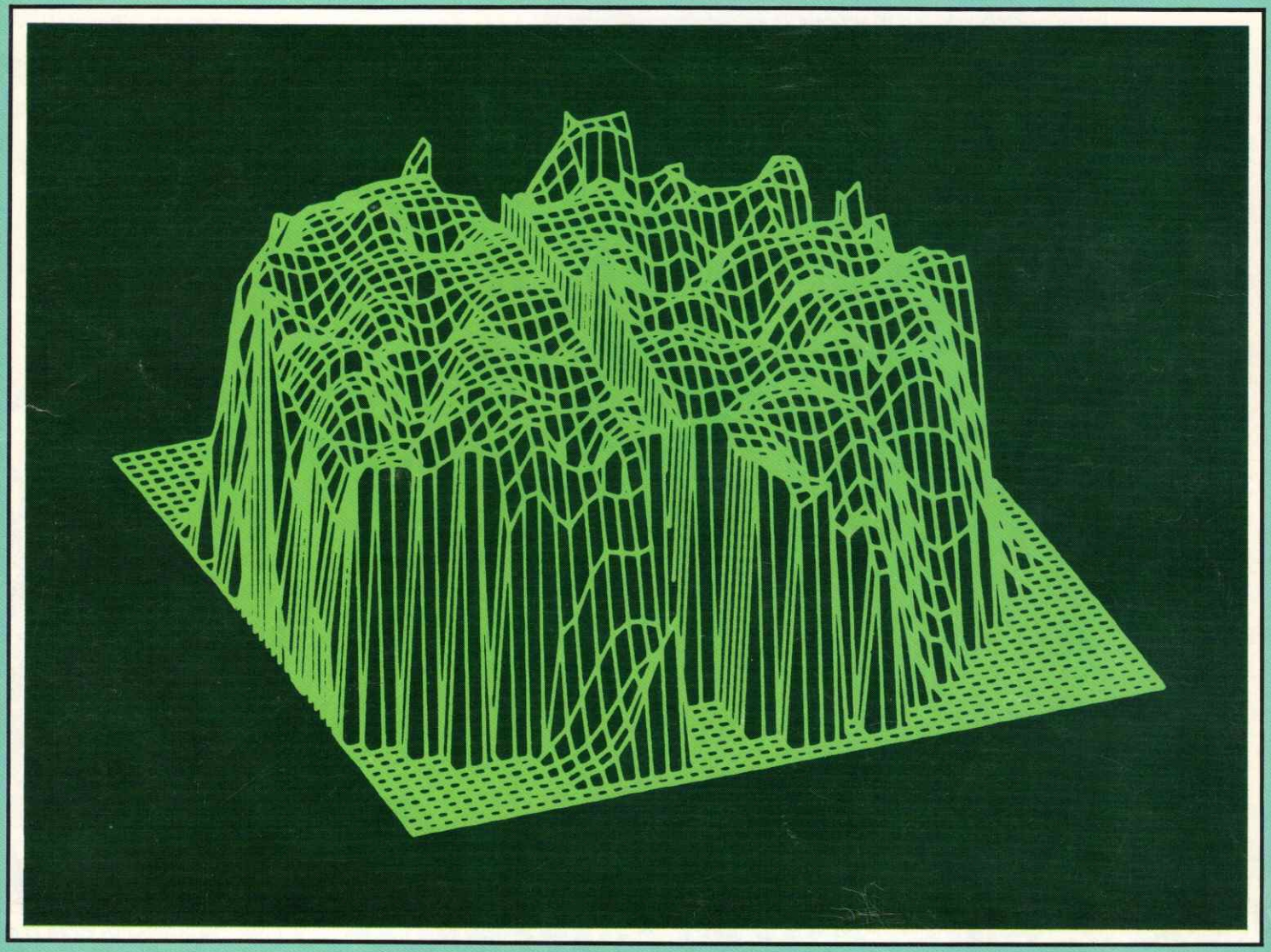

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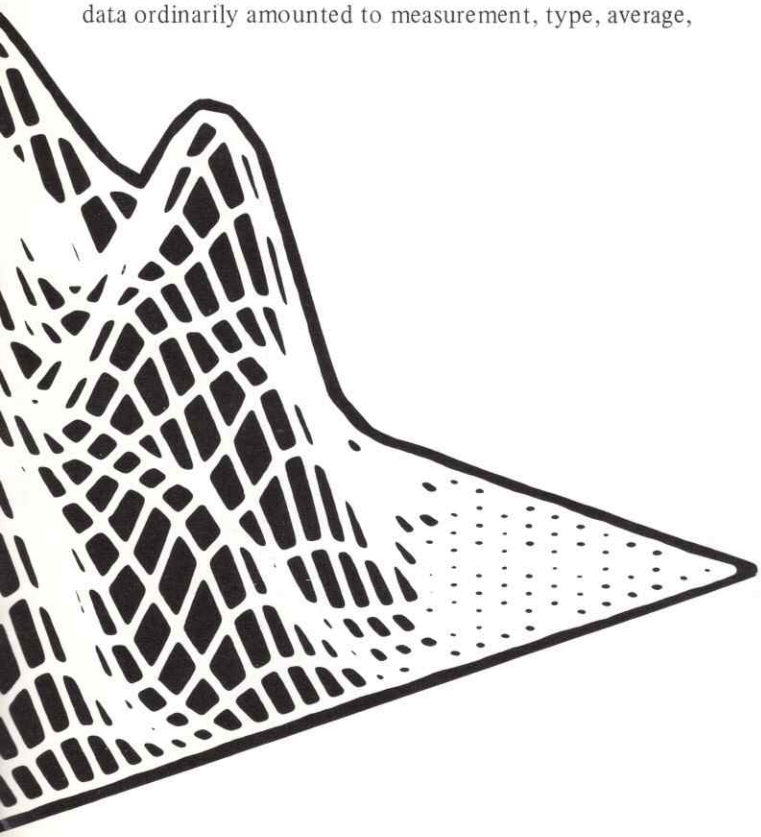
MOUNTAINS OF DATA

data reduction by graphic display

Modern computerized IC test systems can generate vast amounts of quantitative data. One user of such a system calculated that, in a thorough evaluation of a large sample of custom LSI devices, his test system produced enough data to build a stack of line printer fan-fold 42 feet high! Obviously IC test engineers need suitable tools to reduce these "mountains" of data to a more useful, comprehensible form. Without such capability, they could never hope to effectively characterize IC's or IC manufacturing processes. According to Warren Finke, Senior Engineer at Tektronix, Beaverton, OR, a computerized test system which can analyze the data it measures and generate plots on a graphic display terminal represents one of the most efficient ways to attack this problem.

by Gary Wolfe, Assistant Editor

Before computer graphics, how might an engineer reduce test data to a useable form? Jake Tausch, an IC test engineer for Tektronix, recalls testing boxes full of parts on a test system that logged each measurement on paper tape. Tausch would then load the accumulated raw data into a large time-shared computer which reduced the raw data and printed plots on line printer paper. These line printer plots were coarse and difficult to interpret. He notes that such reduced data ordinarily amounted to measurement, type, average, standard deviation and so on. Data presented in this manner frequently made important parametric differences difficult to detect and did not give the test engineer a good "feel" for what was really happening.



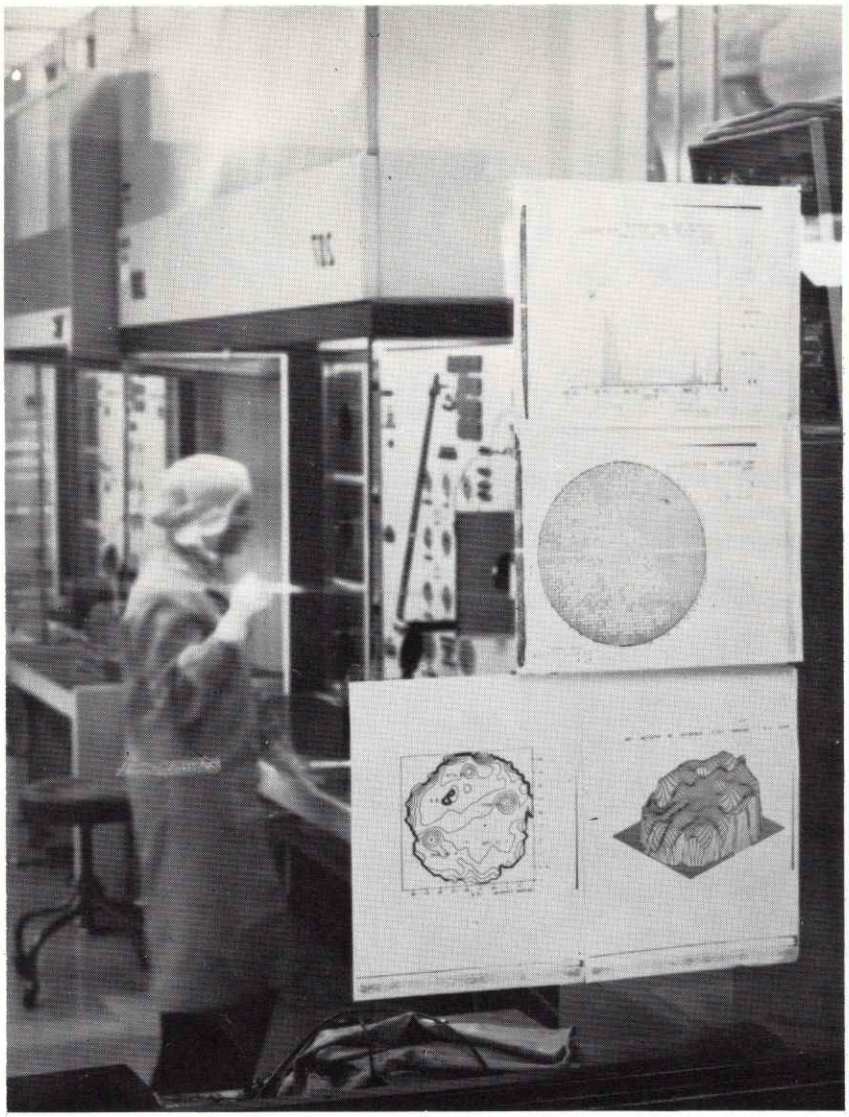
On the other hand, computer graphics, utilized as a data reduction tool, can transform an undigested array of numbers into an easily read and interpreted curve, graph, or special purpose plot. The technique employs a computer to calculate the coordinates of straight line segments called vectors. These vectors are traced on the storage CRT of a graphic display terminal (such as the one incorporated in the Tektronix S-3260 automatic test system). By using many vectors of varying length and orientation, the computer can draw complex graphic displays on the terminal screen.

Plotted between two axes some graphic displays (e.g. shmoo plots, histograms, scatter plots, and log curves) summarize information in two-dimensional figures. Other types of graphic displays reduce information to three-dimensional plots. Test engineers at Tektronix employ both two- and three-dimensional plots to characterize the company's IC devices during development and production phases. Through the use of the calculating power of the computer, the process takes only a few seconds. A companion hard copy unit, interfaced to the graphics terminal provides permanent copies of the display.

drawing the line with histograms

Tausch refers to the histogram as the "real workhorse" of the graphic displays which he employs. A form of bar graph, the histogram scales values of the parameter of interest along the X axis; on the Y, or vertical, axis the scale indicates the number of devices falling into each measured parameter category. The height of the bar illustrates the number of tested devices at a given parametric value.

In the case of Fig 1, the designer of the MOS LSI device shown expected a threshold of about 1.1 volts. Tausch used



Hard copies of graphic displays provide guidance to IC makers.

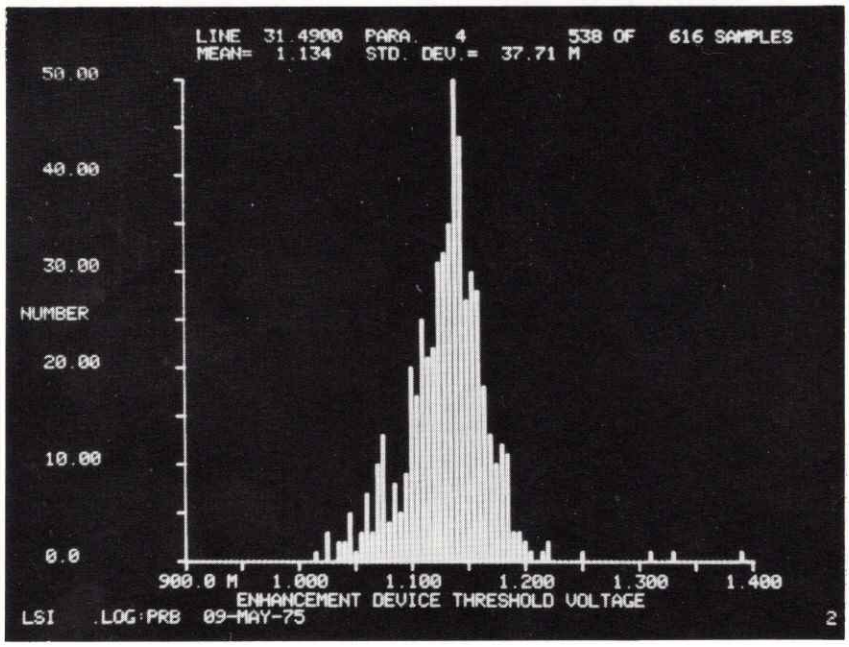


Fig 1 A typical histogram, the "workhorse" of graphic displays.

the test system to probe wafers containing these devices; the system's computer recorded the threshold measurement from each device, calculated vectors and drew the histogram. Almost all of the tested devices exhibited a threshold between 1 volt and 1.2 volts. However, the histogram also shows the threshold centering at around 1.14, not 1.1, volts. This observation suggested that a slight adjustment in the manufacturing process would shift the histogram so that the bars would more tightly group around 1.1 volts. After production engineers made the necessary adjustment, Tausch generated another histogram, using, as the sample, wafers manufactured with the modified process. Through this procedure, the device designer and the process control engineer could "see" the effect of process adjustment on the IC undergoing development.

Sometimes a combination of linear and logarithmic scales in the histogram prove helpful. For example, notes Tausch, when you examine transistors, measurements of current gain (h_{FE}) will vary exponentially with the emitter depth. To obtain a histogram that relates measured gain to process variables, requires a logarithmic X axis, although Y remains linear (Fig 2).

In situations requiring a comparison of histograms, multiple histograms can present all essential data on a single display (Fig 3). A label on the bottom identifies each histogram. The vertical axis serves as the scale for the parameter of interest and, as in the single histogram, the bars graphically show the number of devices exhibiting that parametric value. Finke points out that the multiple histogram allows the viewer to rapidly compare data from different data sets. "We have used multiple histograms to compare results from life tests (where each histogram represented a different time interval), to compare processes (e.g. ion implantation), and to compare vendors. You can learn a lot about a vendor's process control by generating multiple histograms of the parameters critical to your device application. Through such an analysis, you can make informed decisions about which vendors to pick as the primary and secondary sources."

good from bad by wafer map

Keenly interested in yield, IC process engineers can't improve the process until they understand the yield loss mechanisms. To understand such mechanisms, engineers at Tektronix use a form of display called a wafer

map. For example, Jon Schieltz, manager of a Tektronix IC process development group, uses these maps to identify areas on the wafer which exhibit zero yield. "By comparing files of data collected from many wafers, the test system computer draws a composite wafer map that marks die locations, which never yield an acceptable device, with a '+' sign," (Fig 4). He notes, consistently unacceptable dice located in the center of a wafer normally correspond to process or mask defects. On the other hand unacceptable dice located on the periphery usually result from wafer handling problems. The composite wafer map in Fig 5 was generated using data collected from ten wafers containing MOS LSI devices. "In this investigation," he recounts, "we ignored the outliers (die locations around the periphery) and concentrated on a 14% yield loss around the center. The investigation led us to the mask set, which contained flaws in the same die locations identified by the composite wafer maps. Conclusion: if we continued to use this mask set, yield loss would always run at least 14%."

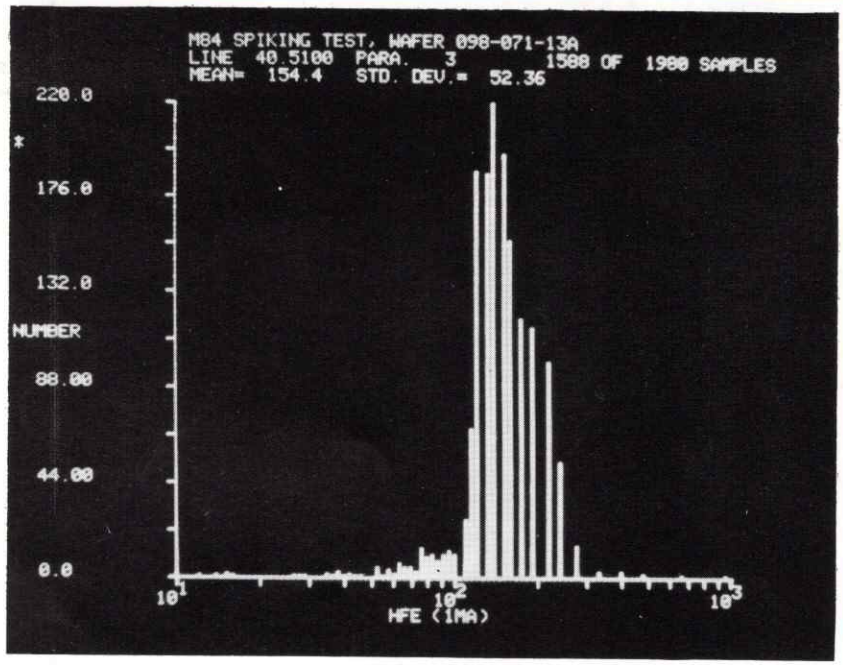


Fig 2 Histogram plotted against a logarithmic X-axis.

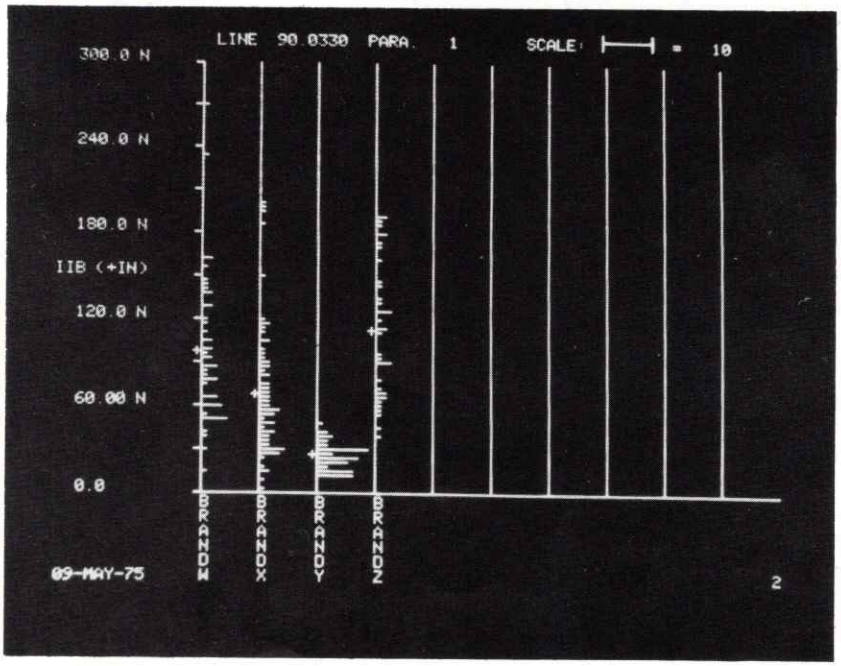


Fig 3 Multiple histogram, a compilation of related process data.

perspectives on 3-D

Useful in process characterization, the three dimensional wafer plot shows how a particular device parameter varies across the wafer. In Fig 6, the plot uses an X-Y grid as the base, each square representing die location. Like the bars in a histogram, the elevation (or height) of the Z axis indicates the quantitative value of the measured parameter (e.g. amplifier gain, as illustrated in Fig 6).

When generating a 3-D plot on a graphic terminal, the operator can adjust the base of the graph, or even take a section out of the middle. In so doing, the operator sets a min-max limit for the z-axis, useful when trying to distinguish minute parametric variations. For example, this procedure permits the terminal to plot a resistivity of 300 ohms, which may vary by only 1/10 ohm. A graph ranging over a z-axis scale of 0-300 ohms would show hardly any variation across the wafer under test. But, a plot from 299 to 301 ohms would permit variations in resistivity of 1/10 ohm to stand out clearly on the screen.

In the application of three-dimensional wafer maps for process development, the employment of special test masks enables measurement of parameters other than circuit response. Such test masks permit the production of a simple device – actually a resistor of one deposited layer – the measurements of which, when graphed in three dimensions, will indicate how well a manufacturing process can put down a particular film.

According to Finke, "Each time the process engineer makes a change, we test sample wafers and instruct the test system computer to plot a three-dimensional wafer plot, one for each wafer and parameter of interest. This plot provides the process engineer with information, which allows a qualitative analysis of the effects of various diffusions, ion implantations, and other process variables."

In a somewhat different application, Schieltz uses the 3-D plot as an aid to determine variations in sheet resistivity. Recalling a comparison of a diffused base versus an implanted base, he notes that the plot of the diffused base looked very lumpy and indicated a variation in diffusion depth or the

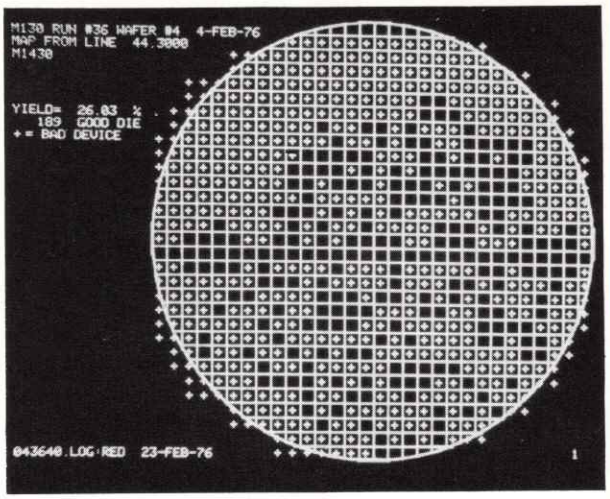


Fig 4 On this wafer map "+" signs denote bad ICs.

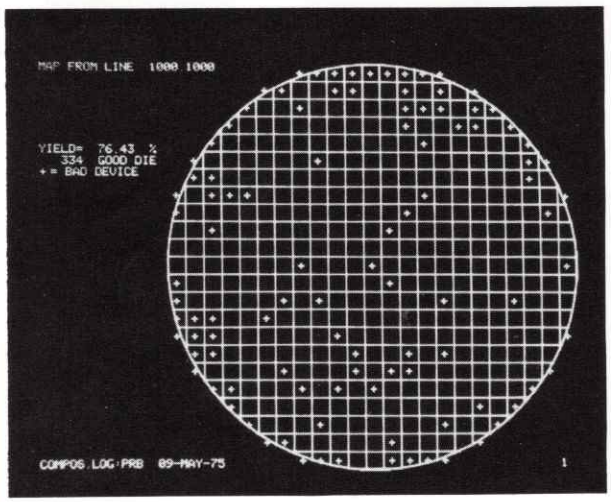


Fig 5 Composite map combines data from ten wafers.

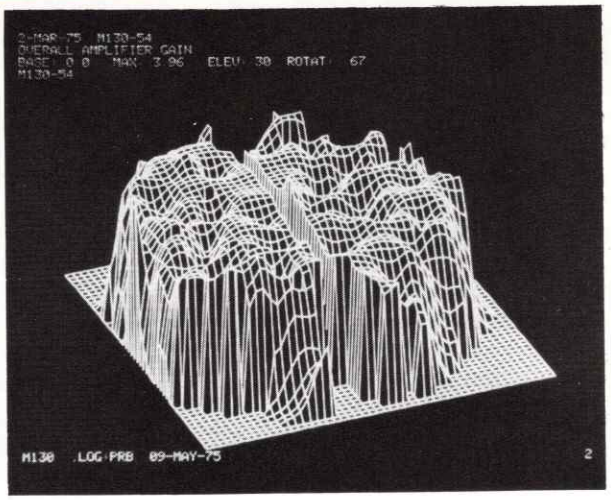


Fig 6 In this 3-D map, the Z-axis denotes gain.

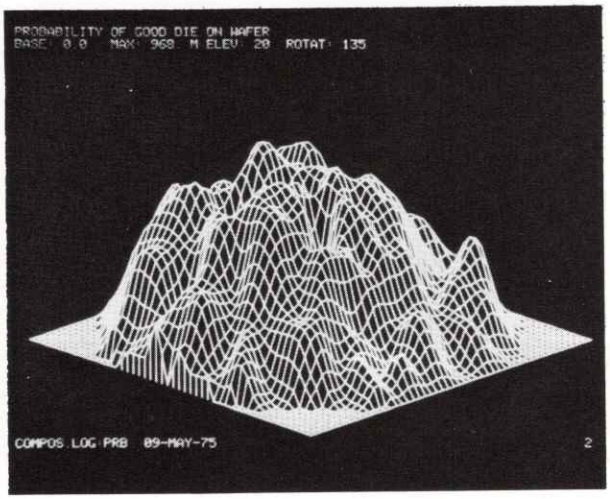


Fig 7 Three-D map to establish probability of good die.

presence of surface contaminants. The implanted base, however, almost resembled a table top, indicative of better sheet resistivity control.

In addition 3-D wafer maps can serve purposes other than the observing of process variations across wafers. Schieltz recently used them while engaged in researching mask alignment problems in microwave ICs. In his technique, Schieltz uses a a special test device in conjunction with the 3-D plots. "Basically the device amounts to a resistor with a center tap aligned to it. This device serves as a voltage divider; the difference in voltage varies proportionally to misalignment.

During the manufacture of wafers containing the test devices, Tektronix employed several different people to align the mask set, each using various alignment keys and techniques. Then, measurement data, collected from each wafer, enabled the test system computer to generate a three-dimensional wafer plot. By comparing the various wafer plots, Schieltz could determine whether the misalignment was a linear shift, rotation or straight runout.

Three dimensional plots also help in the characterization of packaged devices by allowing the test engineer to observe the interaction of three different parameters. "Suppose you want to observe the effects of power supply voltage variations on propagation delay," suggests Tausch. "In this type of three dimensional plot, the X and Y axes represent values of positive and negative power supply voltage respectively. The Z axis indicates the propagation delay in nanosecond increments. In this plot flat areas indicate operating regions where propagation delay remains unaffected by power supply variations; steep slopes indicate operating regions where small variations in the power supplies result in excessive changes in propagation delay."

contour maps — the plane truth

According to Schieltz, three-dimensional plots work well for summary information, but, for detailed information you must use a contour map. In appearance a wafer contour map looks much like the contour maps used in geography to indicate changes in elevation. However, in this case, elevation corresponds to the measured values of the Z axis parameter in a three-dimensional plot. Compare the mountain-like appearance of a three-dimensional wafer plot (Fig 7) with a contour map of the same data (Fig 8). Fig 9 illustrates the detailed information possible when the display terminal enlarges a section of the contour map

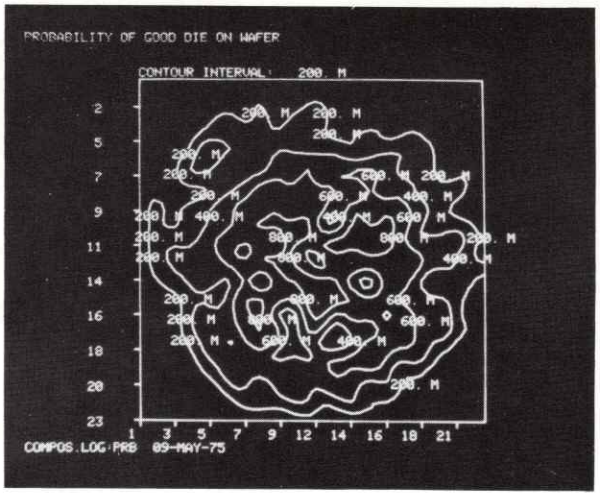


Fig 8 Contour map shows the same data as Fig 7.

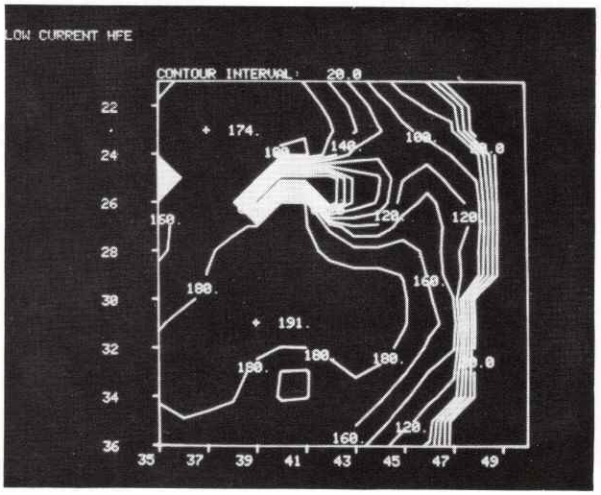


Fig 9 Enlarged section of contour map adds to detail.

on the terminal screen. At this magnification, the test system computer can label the value at each die location.

graphic afterthoughts

Engineers at Tektronix have used graphic data reduction in their IC design and process development work for about a year and a half. "We generally characterize 100% of the first few runs of any new IC," notes Finke, "and with computer graphic displays we can document and communicate our findings. After the developmental phase, we limit our efforts to monitoring the wafer production. We usually keep a copy of the wafer map, recording the locations of the acceptable and unacceptable dice generated from testing each wafer. If the yield drops below our standards, we go back to full characterization until we identify and solve the problem. In this manner, computer graphic displays have played a key role in accelerating the development and production of new IC designs at Tektronix."

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